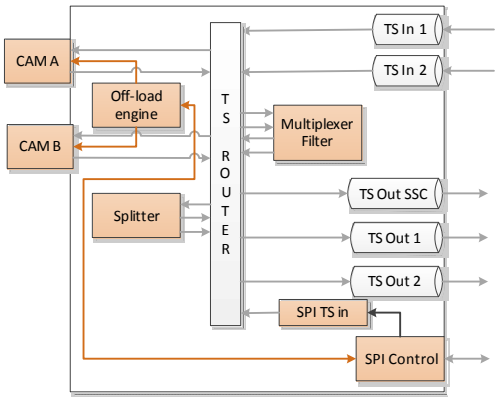
Features

- Support for two DVB-CI and CI+ compliant slots
  - Adapted pin-out for easy routing
  - Full DVB-CI support including interrupt and wait
- Easy interfacing with existing chips
  - Choice of SPI, SDIO, or Ethernet RMII control interfaces
  - Choice of SPI, SDIO, SSC, or RMII MPEG TS output
  - Two serial MPEG TS inputs
- Bus access offload engine
  - Lowers main CPU load
  - Prevents bus lock
  - Efficient use of serial bus (up to 95% useful data in transfer)
- MPEG TS processing capabilities
  - Routing matrix
  - Packet filter
  - Stream multiplexer (CI+ 1.4 compliant)
  - Stream splitter (CI+ 1.4 compliant)
  - IP stream pacing mechanism
  - Adaptive jitter control (experimental)
- Flexible TS input and output interfaces
  - Parallel TS[1], Serial TS, SPI, SDIO, and Ethernet RMII
  - Supports two tuner input streams[2]
  - Supports IP input
  - Supports TS multiplexed output

Default configuration:

- 2 serial MPEG TS inputs
- 2 serial MPEG TS outputs
- 1 Synchronous Serial Port (Packet filter)
- SPI Control port
- Interrupt line

Contact us for other possible configurations



[1] Available on BGA packages only

[2] More input can be supported in BGA packages

RABBITLABS
CI and CI+ Specialists

CAMaLotKS RBL042

Dual slot DVB-CI and CI+ 1.4 CAM Interface for TV Host

1 Description

1.1 General

CAMaLotKS RL042 is a chip that connects two DVB-CI or CI+ compliant CAM slots to an existing chip. CAMaLotKS can be used when the existing chip does not natively support the DVB-CI interface or when the provided support is not sufficient (only single slot, no handling of CI+1.4 multi-stream, etc.)

1.2 Serial MPEG TS Input

The interface has two serial TS inputs. Each input supports clock rates up to 100MHz.

1.3 SPI MPEG TS Input

This input can be used as an auxiliary input to feed packets to the system from the main CPU. It supports streaming speed of up to 30 MHz, but the bandwidth has to be shared with the command stream. It will normally be connected to the tuner.

1.4 Serial MPEG TS Output

This output can be used to stream data back to the main chip after processing by the CAM. It can either use a fixed configurable clock speed or re-use the input TS clock. An output buffers guarantees that output packets do not contain holes.

1.5 Synchronous Serial MPEG TS Output

This output is intended to stream filtered packets to the main CPU. The output format is synchronous serial port, output speed and format are configurable to match the target system. An output buffer guarantees that output packets do not contain holes.

1.6 MPEG TS multiplexer and filter

The TS Multiplexer and filter can be used to mix together two MPEG streams to create a single CI+1.4 compliant multi-stream. PIDs can be selected from each stream to reduce final bandwidth. Additionally, the MPEG filter can extract specific PIDs and send them over the synchronous serial port. This can be used if the main chip used in the system lacks MPEG TS section filtering capabilities.

1.7 MPEG TS splitter

The MPEG TS Splitter splits the CI+1.4 compliant multi-stream into two single stream. It can also fix jitter introduced by the multiplexing process.

1.8 Command Interface offload engine

The command interface offload engine is controlling the command interface to CAM. It receives a batch of commands from the main chip and executes them. The result is returned in a buffer which can be read at convenience. By executing large batches of instructions in stand-alone mode, this block dramatically reduces the load on the main CPU for handling CAM communication. Thanks to an efficient implementation, transfer rates up to 2MB/s can be achieve over a 30Mhz SPI interface.

1.9 SPI Control interface

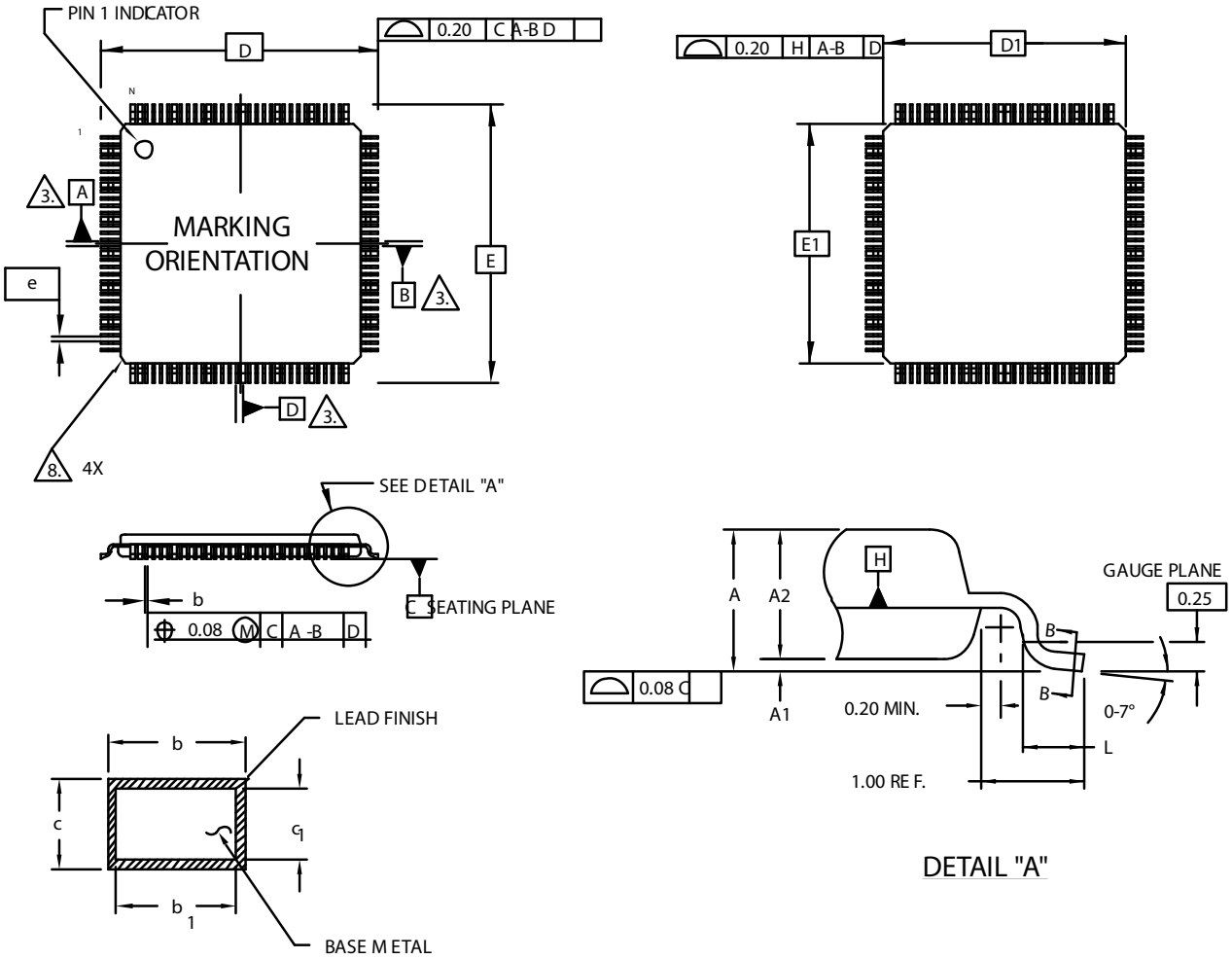
The SPI control interface is a standard SPI slave interface with an interrupt line. It can use a clock up to 30Mhz.

2 Pin assignment (default)

Pin	Function	I/O
1	LV_MOSTRT2	Input
2	LV_MOSTRT1	Input
3	LV_MDO1_0	Input
4	A0	Output
5	A1	Output
6	A2	Output
7	VCC	
8	VSS	
9	LV_MOVAL2	Input
10	LV_MOVAL1	Input
11	LV_MOCLK2	Input
12	LV_MOCLK1	Input
13	LV_/IREQ2	Input
14	LV_/IREQ1	Input
15	NC	
16	VCC	
17	NC	
18	VSS	
19	LV_MDO2_7	Input
20	LV_MDO1_7	Input
21	/REG	Output
22	A3	Output
23	A4	Output
24	/WAIT2	Input
25	/WAIT1	Input
26	A5	Output
27	A6	Output
28	RESET2	Output
29	VSS	
30	VCC	
31	NC	
32	RESET1	Output
33	MDI2_7	Output
34	A7	Output
35	MDI2_6	Output
36	VCC	
37	VCC	
38	NC	Output
39	MDI1_7	Output
40	A12	Output
41	MDI1_6	Output
42	MDI2_5	Output
43	MICLK1	Output
44	MICLK2	Output
45	MIVAL2	Output
46	VSS	
47	MDI2_4	Output
48	MDI1_5	Output
49	MIVAL1	Output
50	MDI1_4	Output
51	VCC	
52	/WE	Output
53	VSS	
54	MDI1_3	Output
55	MDI2_3	Output
56	MDI1_2	Output
57	MDI2_2	Output
58	MDI2_1	Output
59	A13	Output
60	A8	Output
61	MDI1_1	Output
62	A14	Output
63	NC	
64	VSS	
65	MDI2_0	Output
66	VCC	
67	MDI1_0	Output
68	MISTRT1	Output
69	MISTRT2	Output
70	A9	Output
71	/IOWR	Output
72	VCC	

Pin	Function	I/O
73	/IORD	Output
74	/OE	Output
75	A11	Output
76	A10	Output
77	/CE21	Output
78	/CE11	Output
79	VCC	
80	VSS	
81	LV_MDO2_6	Input
82	LV_MDO1_6	Input
83	LV_MDO2_5	Input
84	LV_MDO1_5	Input
85	LV_MDO2_4	Input
86	LV_MDO1_4	Input
87	NC	
88	VCC	
89	NC	
90	VSS	
91	LV_MDO2_3	Input
92	LV_MDO1_3	Input
93	CI_DATA_DIR	Output
94	CI_DATA_EN	Output
95	LV_CI_D2	BIDIR
96	LV_CI_D1	BIDIR
97	LV_CI_D0	BIDIR
98	LV_CI_D7	BIDIR
99	LV_CI_D6	BIDIR
100	LV_CI_D5	BIDIR
101	VSS	
102	VCC	
103	NC	
104	LV_CI_D4	BIDIR
105	LV_CI_D3	BIDIR
106	CS	Input
107	MISO	Output
108	VCC	
109	IT	Input
110	MOSI	Input
111	SPCK	Input
112	SSC_RF	Output
113	SSC_RK	Output
114	STSOUT2_VAL	Output
115	STSOUT2_STRT	Output
116	VSS	
117	STSOUT2_DAT	Output
118	VCC	
119	SSC_RD	Output
120	NC	
121	STSOUT2_CLK	Output
122	STSOUT1_VAL	Output
123	VCC	
124	VSS	
125	STSOUT1_STRT	Output
126	STSOUT1_DAT	Output
127	STSOUT1_CLK	Output
128	STSIN2_VAL	Input
129	NC	
130	STSIN2_STRT	Input
131	STSIN2_DAT	Input
132	STSIN2_CLK	Input
133	STSIN1_VAL	Input
134	VSS	
135	VCC	
136	STSIN1_STRT	Input
137	STSIN1_DAT	Input
138	STSIN1_CLK	Input
139	LV_MDO2_2	Input
140	LV_MDO2_1	Input
141	LV_MDO2_0	Input
142	LV_MDO1_1	Input
143	LV_MDO1_2	Input
144	VCC	

3 Package drawings



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1982.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
5. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15 MM.
6. SECTION B-B:
   THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 MM FROM THE LEAD TIP.
7. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

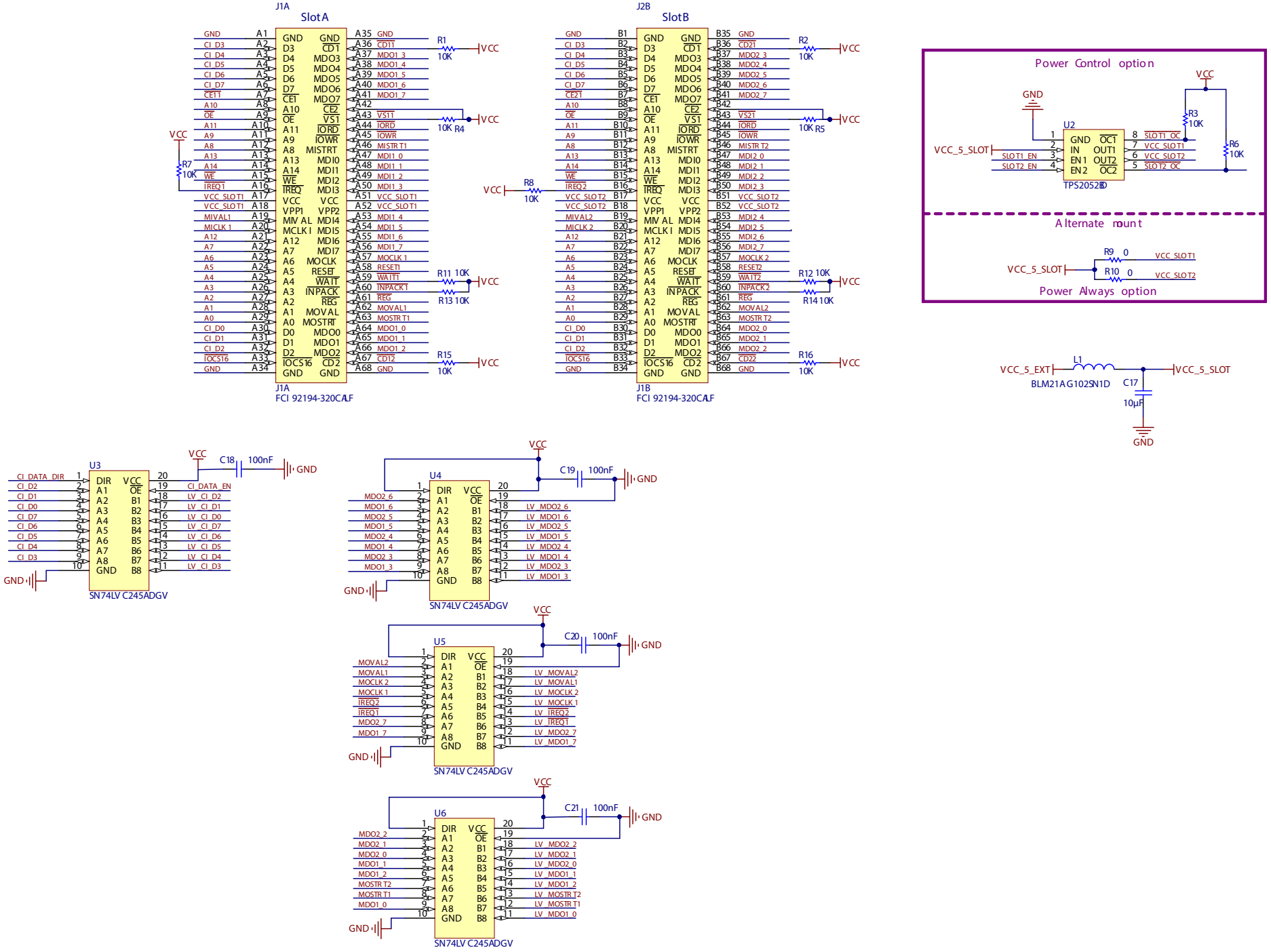
SYMBOL	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	22.00 BSC		
D1	20.00 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
N	144		
e	0.50 BSC		
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	0.15	0.20
c1	0.09	0.13	0.16

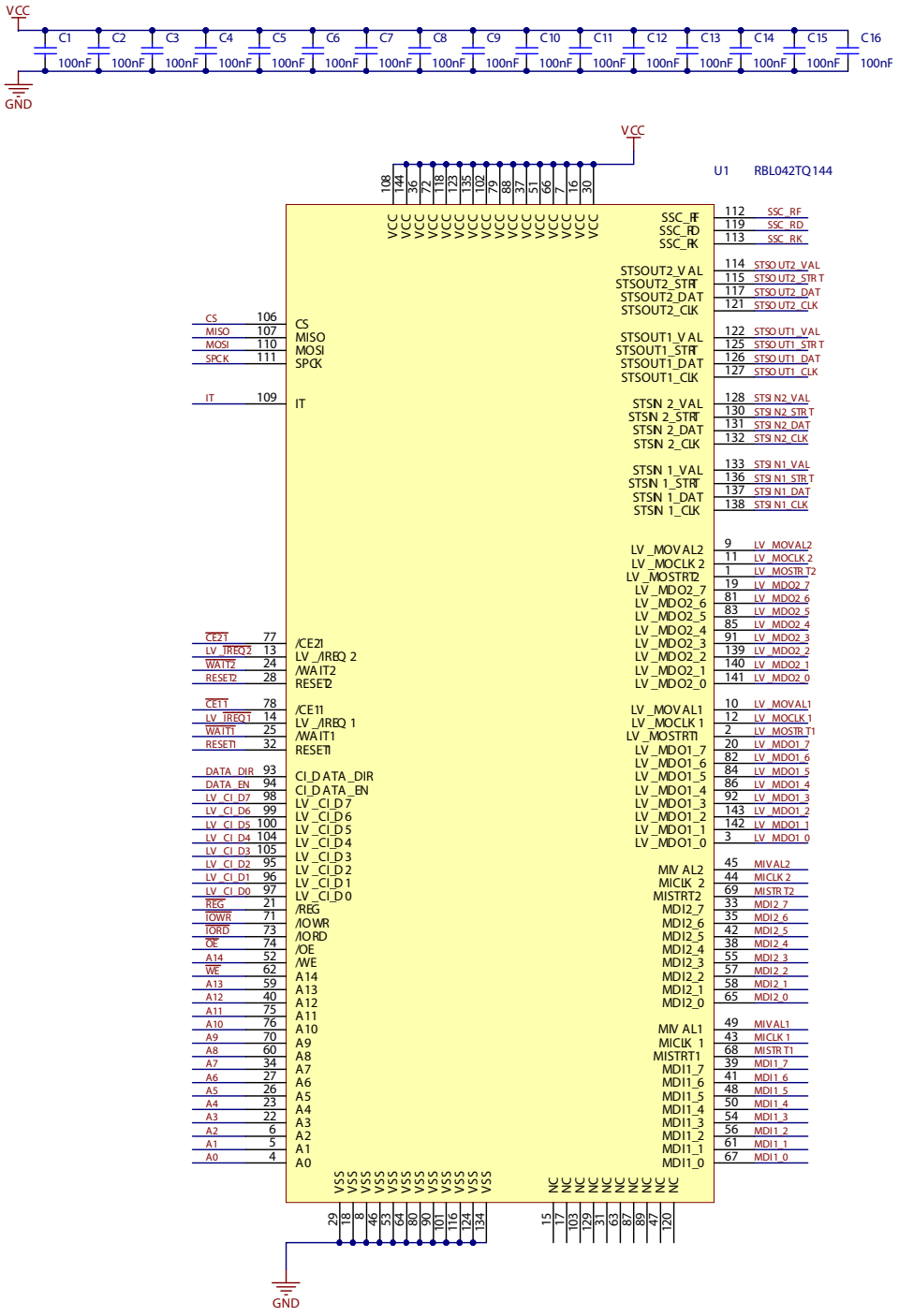
4 Electrical characteristics

	Min	Max
Vcc	2.5V	3.45V
Vin	-0.5V	3.45V
Storage temperature	-55°C	125°C
Junction temperature	0°C	85°C

5 Typical application

Since CAMaLotKS does not use 5V tolerant interface, signals coming from CAM must be buffered to avoid damaging the chip.


J1A
Slot A
J1A
FCI 92194-320CALF
J2B
Slot B
J1B
FCI 92194-320CALF
Power Control option
Alternate mount
Power Always option
TPS2052BD
SN74LV C245ADGV
SN74LV C245ADGV
SN74LV C245ADGV
SN74LV C245ADGV
BLM21AG102SN1D
VCC_5_EXT
VCC_5_SLOT
10µF
100nF


VCC
C1 100nF
C2 100nF
C3 100nF
C4 100nF
C5 100nF
C6 100nF
C7 100nF
C8 100nF
C9 100nF
C10 100nF
C11 100nF
C12 100nF
C13 100nF
C14 100nF
C15 100nF
C16 100nF
GND
U1 RBL042TQ144
108 144 36 72 118 123 135 102 79 88 37 51 66 7 16 30
VCC
CS 106
MISO 107
MOSI 110
SPCK 111
IT 109
CE2I 77
LV_IREQ2 13
WAIT2 24
RESET2 28
CE1I 78
LV_IREQ1 14
WAIT1 25
RESET1 32
DATA_DIR 93
DATA_EN 94
LV_CI_D7 98
LV_CI_D6 99
LV_CI_D5 100
LV_CI_D4 104
LV_CI_D3 105
LV_CI_D2 95
LV_CI_D1 96
LV_CI_D0 97
REG 21
IOWR 71
IORD 73
OE 74
A14 52
WE 62
A13 59
A12 40
A11 75
A10 76
A9 70
A8 60
A7 34
A6 27
A5 26
A4 23
A3 22
A2 6
A1 5
A0 4
SSC_RF 112
SSC_RD 119
SSC_RK 113
STSOUT2_VAL 114
STSOUT2_STRT 115
STSOUT2_DAT 117
STSOUT2_CLK 121
STSOUT1_VAL 122
STSOUT1_STRT 125
STSOUT1_DAT 126
STSOUT1_CLK 127
STSIN2_VAL 128
STSIN2_STRT 130
STSIN2_DAT 131
STSIN2_CLK 132
STSIN1_VAL 133
STSIN1_STRT 136
STSIN1_DAT 137
STSIN1_CLK 138
LV_MOVAL2 9
LV_MOCLK2 11
LV_MOSTRT2 1
LV_MDO2_7 19
LV_MDO2_6 81
LV_MDO2_5 83
LV_MDO2_4 85
LV_MDO2_3 91
LV_MDO2_2 139
LV_MDO2_1 140
LV_MDO2_0 141
LV_MOVAL1 10
LV_MOCLK1 12
LV_MOSTRT1 2
LV_MDO1_7 20
LV_MDO1_6 82
LV_MDO1_5 84
LV_MDO1_4 86
LV_MDO1_3 92
LV_MDO1_2 143
LV_MDO1_1 142
LV_MDO1_0 3
MIVAL2 45
MICLK2 44
MISTRT2 69
MDI2_7 33
MDI2_6 35
MDI2_5 42
MDI2_4 38
MDI2_3 55
MDI2_2 57
MDI2_1 58
MDI2_0 65
MIVAL1 49
MICLK1 43
MISTRT1 68
MDI1_7 39
MDI1_6 41
MDI1_5 48
MDI1_4 50
MDI1_3 54
MDI1_2 56
MDI1_1 61
MDI1_0 67
VSS 29 18 8 46 53 64 80 90 101 116 124 134
NC 15 17 103 129 31 63 87 89 47 120
GND